CBCS SCHEME

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15CS72

Seventh Semester B.E. Degree Examination, Dec.2023/Jan.2024
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain Uniform Memory Access (UMA) and Non-Uniform Memory Access (NUMA) multiprocessor models. **(06 Marks)**

b. Define the various types of data dependence. **(05 Marks)**

c. Draw the dependence graph showing both data and resource dependence for the following code segment :

$P_1 : C = D \times E$
$P_2 : M = G + C$
$P_3 : A = B + C$
$P_4 : C = L + M$
$P_5 : F = G \div E$ **(05 Marks)**

OR

2 a. Explain the topologies of the following static connection networks, in terms of network parameters :

(i) Linear array
(ii) Ring.
(iii) Barrel shifter.
(iv) Mesh. **(08 Marks)**

b. Explain Flynn's classification of computer architectures, with neat block diagrams. **(08 Marks)**

Module-2

3 a. Distinguish between RISC and CISC processor architectures with the help of block diagram. Also compare the architectural characteristics of the same. **(10 Marks)**

b. Explain in detail, hierarchical memory technology. **(06 Marks)**

OR

4 a. Consider the design of a three level memory hierarchy with the following specifications ;

Memory level	Access time	Capacity	Cost / K byte
Cache	$t_1 = 25$ ns	$S_1 = 512$ kB	$C_1 = \$ 0.12$
Main memory	t_2 = unknown	$S_2 = 32$ MB	$C_2 = \$ 0.02$
Disk array	$t_3 = 4$ ms	S_3 = unknown	$C_3 = \$ 0.00002$

(i) Compute S_3, if the total cost of the memory hierarchy is upper_bounded by \$ 1500.
(ii) Compute t_2, if effective memory access time t = 850 nS with a cache hit ratio $h_1 = 0.98$ and $h_2 = 0.99$ in main memory. **(08 Marks)**

b. What is page replacement? Define the various page replacement policies. **(08 Marks)**

Module-3

5 a. With neat block diagrams, explain bus arbitration schemes. **(10 Marks)**

b. List the various block mapping schemes for cache memory. Explain any one in detail. **(06 Marks)**

OR

6 a. Explain in detail, the following mechanisms for instruction pipelining :
(i) Prefetch buffers.
(ii) Internal data forwarding **(08 Marks)**

b. Consider the following pipeline reservation table :

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

(i) What are the forbidden latencies?
(ii) Draw the state transition diagram.
(iii) List all the simple and greedy cycles.
(iv) Compute Minimal Average Latency (MAL)
(v) Determine the throughput using MAL. **(08 Marks)**

Module-4

7 a. Explain in detail, write invalidate and write update cache coherence protocols for write through caches. **(08 Marks)**

b. Explain the format of message used in a message passing network. Also differentiate between store-and-forward routing and wormhole routing. **(08 Marks)**

OR

8 a. Explain the various prefetching techniques used in shared virtual memory. **(04 Marks)**

b. Define the following :
(i) Sequential consistency
(ii) Processor consistency.
(iii) Weak consistency
(iv) Release consistency. **(04 Marks)**

c. Explain the various context-switching policies adopted in multithreaded architectures. **(08 Marks)**

Module-5

9 a. Define the two basic mechanisms used for inter process communication. **(04 Marks)**

b. Explain any four language features for parallel programming. **(08 Marks)**

c. Illustrate spin locks and suspend locks used for protected access of shared variables. **(04 Marks)**

OR

10 a. Define loop unrolling. Illustrate the same with a suitable example. **(05 Marks)**

b. With a state transition diagram, explain 2 bit branch predictor. **(05 Marks)**

c. Explain Tomasulo's algorithm. **(06 Marks)**

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